Amendments to the Claims

1. (Amended) An interface for transferring data from a real-time data transfer system to a signal processing unit comprising:

a circular buffer having an input configured to receive data samples from the real-time data transfer system and to periodically send data samples received from the real-time data transfer system to the signal processing unit when the signal processing unit accepts a transfer, wherein the data is stored and transferred according to a first-in, first-out operational protocol; and

a first counter circuit communicating with the signal processing unit and the data transfer system and configured to increment for each data sample sent to the circular buffer from the data transfer system and decrement for each data sample sent to the signal processing unit from the circular buffer, where the counter circuit is configured to count beyond the physical range of the buffer to account for data samples transferred through the circular buffer;

a second circular buffer having an input and an output configured to receive data samples from the signal processing unit and to send data samples to the real-time data transfer system when the data is available;

a second counter circuit communicating with the second circular buffer and configured to increment each time a data sample is received by the second circular buffer from the signal processing unit and decrement each time a data sample is sent from the second circular buffer to the data transfer system, where the counter is configured to count beyond the physical range of the buffer; and

a switch communicating with the second counter circuit and the data transfer system.

2. (previously presented) An interface according to Claim 1, wherein the counter circuit has a programmable threshold and is configured to generate an interrupt to the signal processing unit when the counter passes the threshold.

3. (previously presented) An interface according to Claim 2, wherein the counter is configured to send a subsequent interrupt only after a prior interrupt is acknowledged by the signal processing unit.

4. (previously presented) An interface according to Claim 1, wherein the signal processing unit polls the counter periodically to determine the availability of data samples.

5. Cancel Claim 5.

6. (Previously Cancelled).

7. (Amended) An data transfer device for transferring data from a real-time data transfer system to a signal processor comprising:

buffer means configured to store and transfer data samples between the data transfer system and the processor in a synchronized manner, such that the number of receive samples transferred is substantially equal to the number of transmit samples transferred;

counter means configured to account for data transferred through the buffer means, where the counter means is further configured to count beyond the physical length of the buffer; and

wherein the counter means includes interrupt means configured to send a signal to the signal processor when the counter means increments beyond a first threshold, to receive an acknowledgment signal from the signal processing unit to acknowledge an interrupt signal sent by the counter means and to send a subsequent a interrupt signal only after a prior interrupt signal has been acknowledged.

8. Cancel Claim 8.

9. An interface according to Claim 7, wherein the signal processor periodically polls the counter means to determine the availability of data samples.

10. (Amended) A modem for communicating on a real-time data transfer system comprising:

a signal processor for processing data;

means for converting an analog signal received by the buffer to an digital signal readable by the processor and vice versa;

buffer means configured to store and transfer data samples between the data transfer system and the processor in a synchronized manner, such that the number of receive samples transferred is substantially equal to the number of transmit samples transferred; and

counter means configured to account for data transferred through the buffer means to the signal processor , where the counter means is further configured to count beyond the physical length of the buffer;

wherein the counter means includes interrupt means configured to send a signal to the signal processor when the counter means increments beyond a first threshold, to receive an acknowledgment signal from the signal processing unit to acknowledge an interrupt signal sent by the counter means and to send a subsequent a interrupt signal only after a prior interrupt signal has been acknowledged.

11. (previously presented) An modem according to Claim 10 further comprising means for sending a null signal when data is not ready to be transferred from the buffer means to the data transfer system.

12. (previously presented) An modem according to Claim 10, wherein the most significant bit of the counter means is a sticky bit and is configured to retain a digital logic one in the event of an overflow of the counter and is configured to lose the digital logic one when the counter is subsequently decremented as a result of the signal processing unit reading data from the first buffer means.

13. Cancel Claims 13.

14 (Previously Cancelled)

15. Cancel Claims 15-17.

18. (Amended) An interface for transferring data from a real-time data transfer system to a signal processing unit comprising:

a circular buffer having an input configured to receive data samples from the real-time data transfer system and to send data samples received from the real-time data transfer system to the signal processing unit when the signal processing unit accepts a transfer, wherein the data is stored and transferred according to a first-in, first-out operational protocol; and

a first counter circuit communicating with the signal processing unit and the data transfer system and configured to increment for each data sample sent to the circular buffer from the data transfer system and decrement for each data sample sent to the signal processing unit from the circular buffer, where the counter circuit is configured to count beyond the physical range of the buffer to account for data samples transferred through the circular buffer;

a second circular buffer having an input and an output configured to receive data samples from the signal processing unit and to send data samples to the real-time data transfer system when the data is available;

a second counter circuit communicating with the second circular buffer and configured to increment each time a data sample is received by the second circular buffer from the signal processing unit and decrement each time a data sample is sent from the second circular buffer to the data transfer system, where the counter is configured to count beyond the physical range of the buffer; and

a switch communicating with the second counter circuit and the data transfer system.

19. (Amended) An interface according to Claim 10 ~~18~~, wherein the counter circuit has a programmable threshold and is configured to generate an interrupt to the signal processing unit when the counter passes the threshold, and wherein the conter means further includes

a first counter circuit communicating with the signal processing unit and the data transfer system and configured to increment for each data sample sent to the circular buffer from the data transfer system and decrement for each data sample sent to the signal processing unit from the circular buffer, where the counter circuit is configured to count beyond the physical range of the buffer to account for data samples transferred through the circular buffer; and

a second counter circuit communicating with the second circular buffer and configured to increment each time a data sample is received by the second circular buffer from the signal processing unit and decrement each time a data sample is sent from the second circular buffer to the data transfer system, where the counter is configured to count beyond the physical range of the buffer; and

a switch communicating with the second counter circuit and the data transfer system.

20. (Previously Presented) An interface according to Claim 19, wherein the counter is configured to send a subsequent interrupt only after a prior interrupt is acknowledged by the signal processing unit.

21. (Previously Presented) An interface according to Claim 18, wherein the signal processing unit polls the counter to determine the availability of data samples.

22. (Previously Presented) An interface according to Claim 18, wherein the signal processing unit polls the counter periodically to determine the availability of data samples.

23. Cancel Claim 23.